

FIG. 1

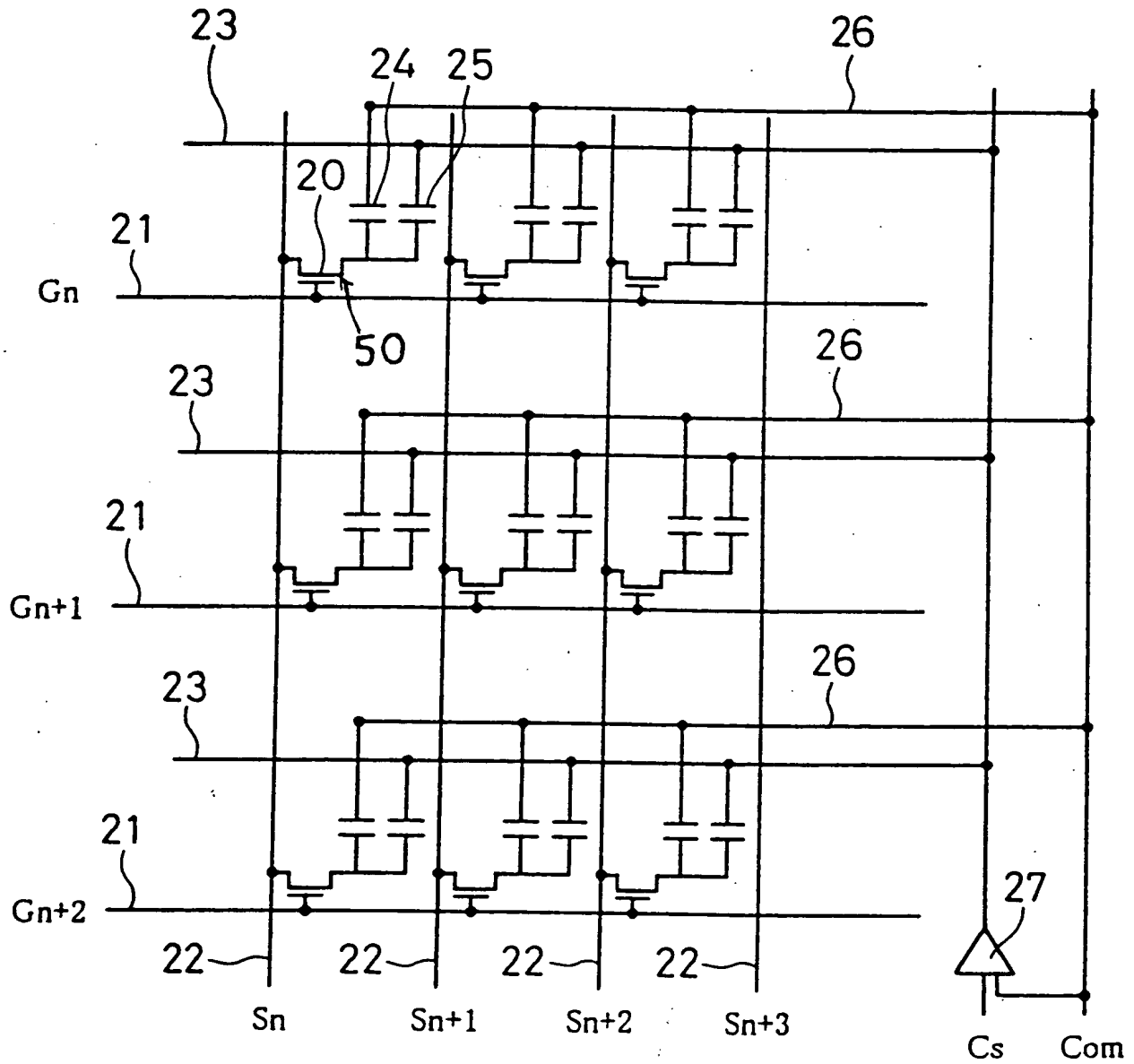
19

FIG. 2A

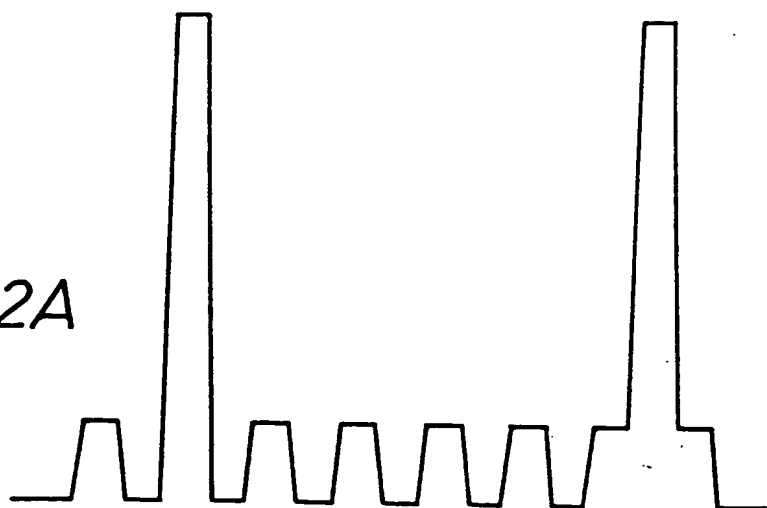


FIG. 2B

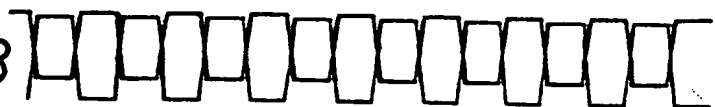


FIG. 2C



FIG. 2D

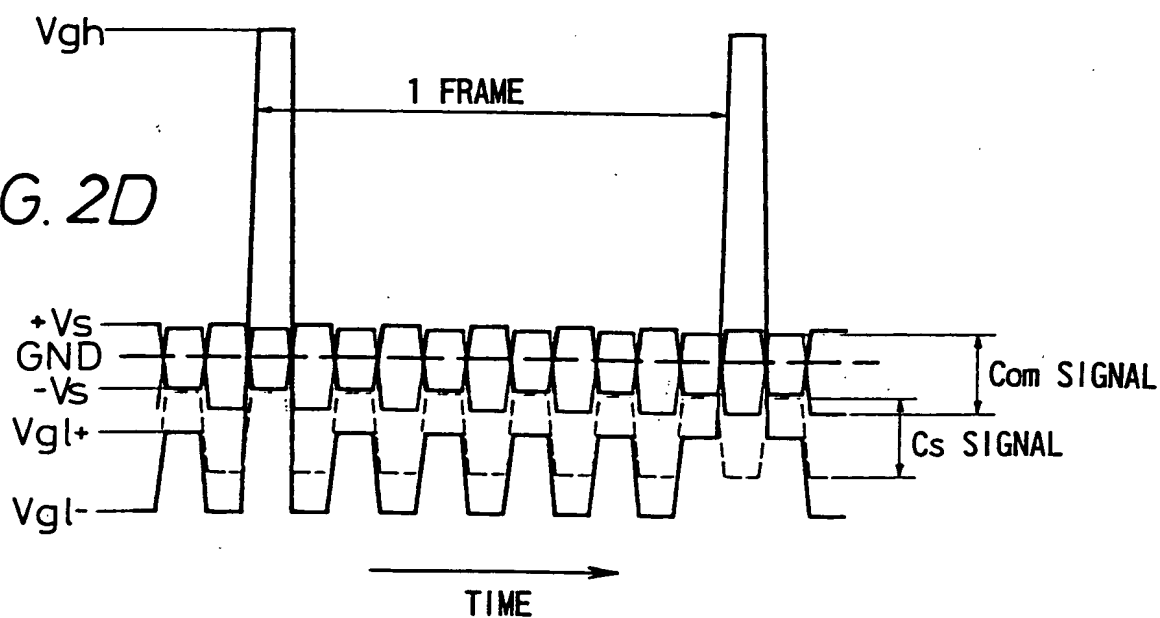


FIG. 3

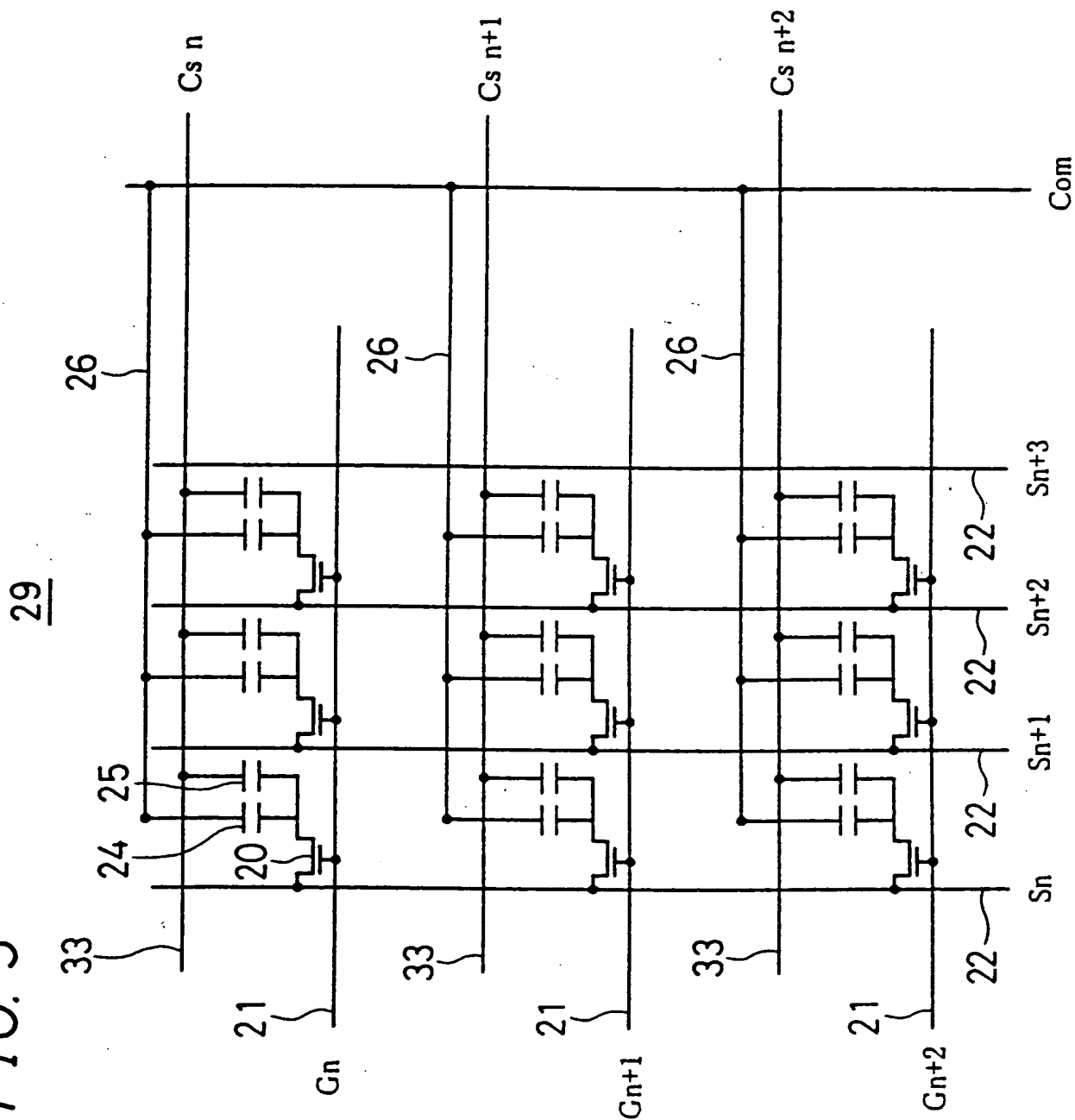


FIG. 4A

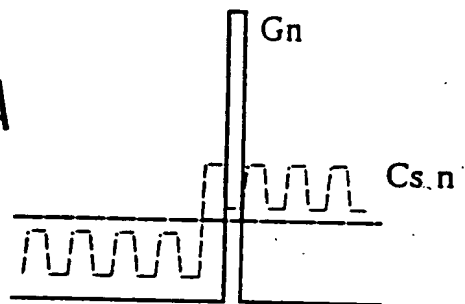


FIG. 4B

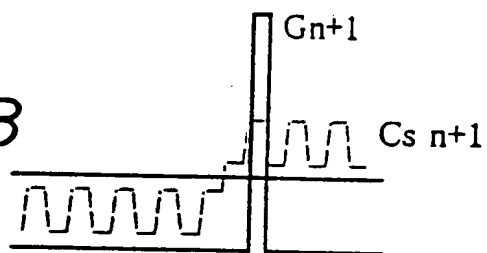
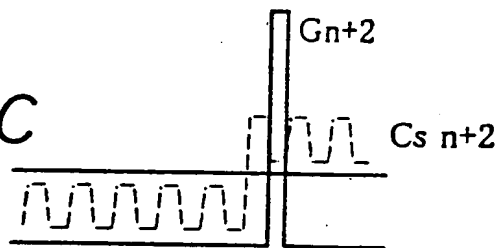
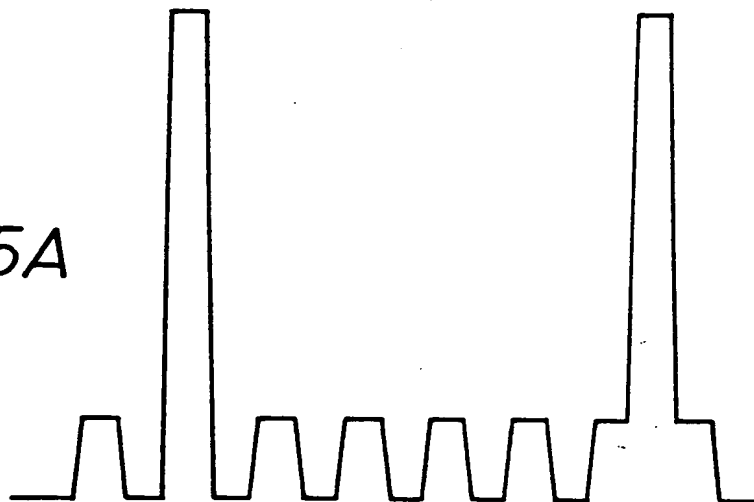


FIG. 4C



→  
TIME

FIG. 5A



*FIG. 5B*



FIG.5C

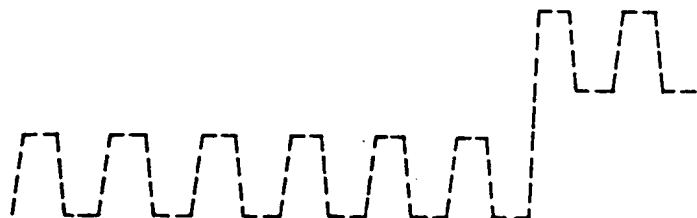


FIG. 5D

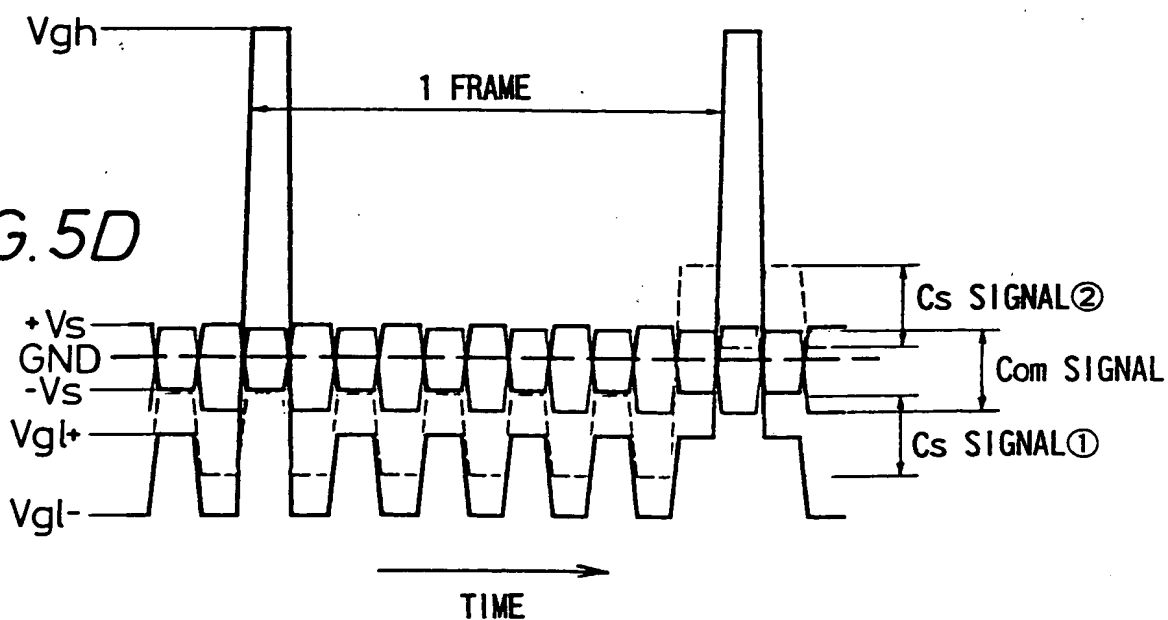


FIG. 6

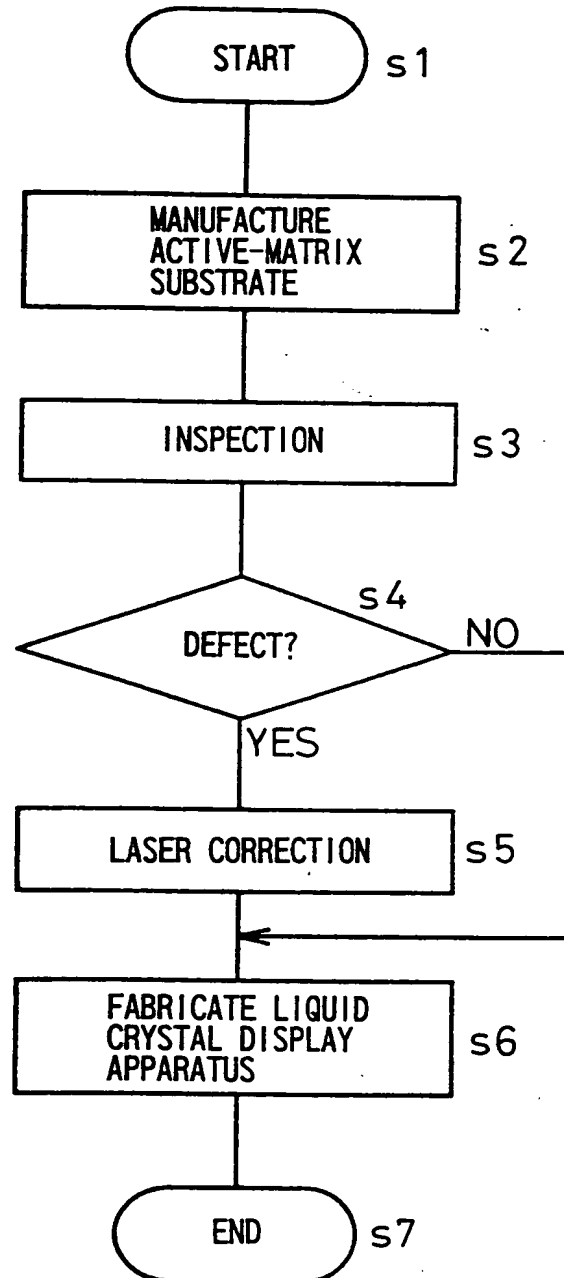
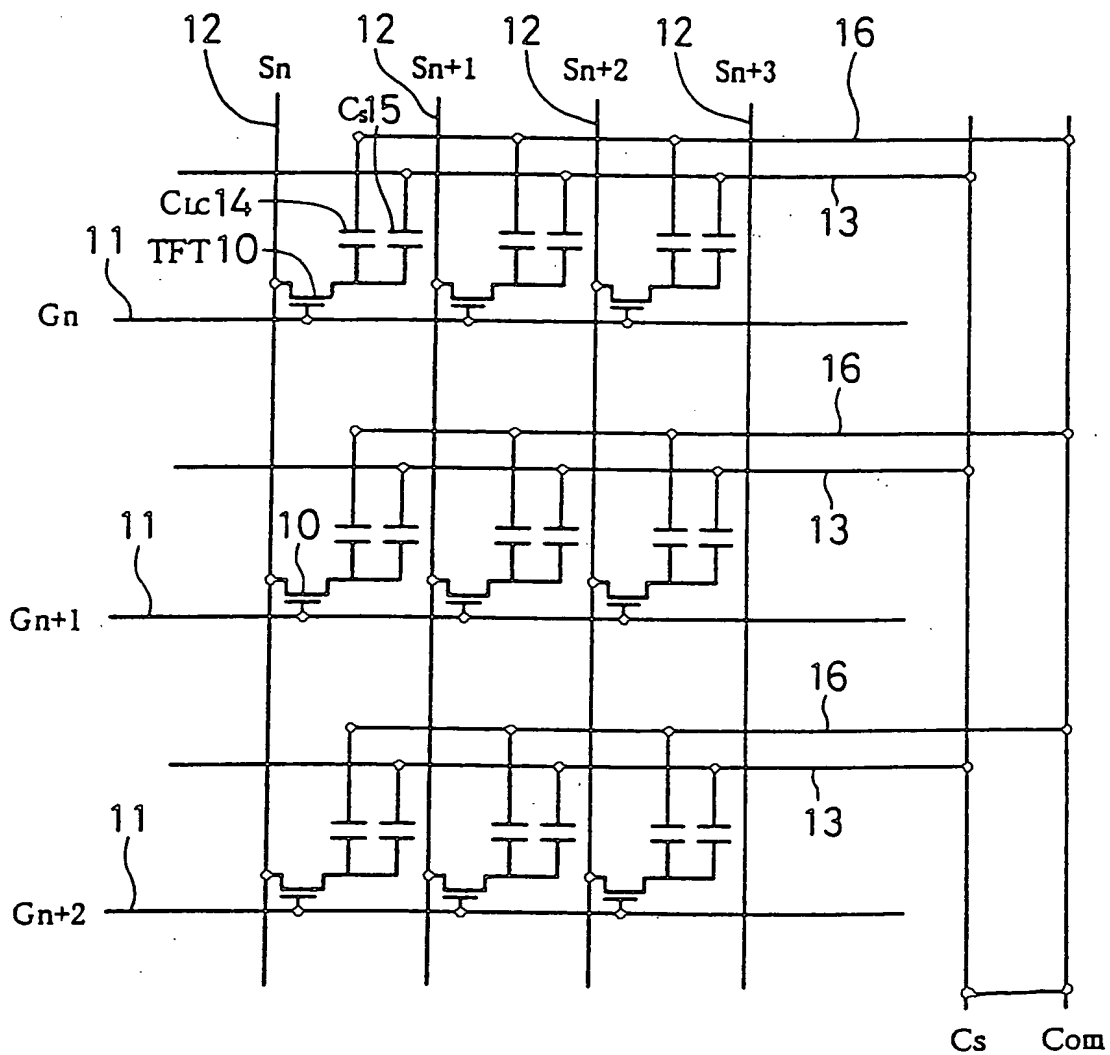
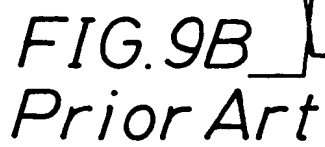




FIG. 8 Prior Art





[illegible]

Timing diagram for the 9C-Art device. The diagram shows the relationship between various signals over time. The signals are:

- Vgh**: High voltage signal, shown as a pulse at the start of the frame.
- +Vs**: Positive supply voltage, shown as a constant high level.
- GND**: Ground, shown as a constant low level.
- Vs**: Negative supply voltage, shown as a constant low level.
- Vgl+**: Gate voltage, shown as a series of pulses during the frame.
- Vgl-**: Gate voltage, shown as a series of pulses during the frame.

The diagram indicates a duration of **1 FRAME** and a **Com SIGNAL (= Cs SIGNAL)** which is the difference between Vgl+ and Vgl-.

FIG. 10A

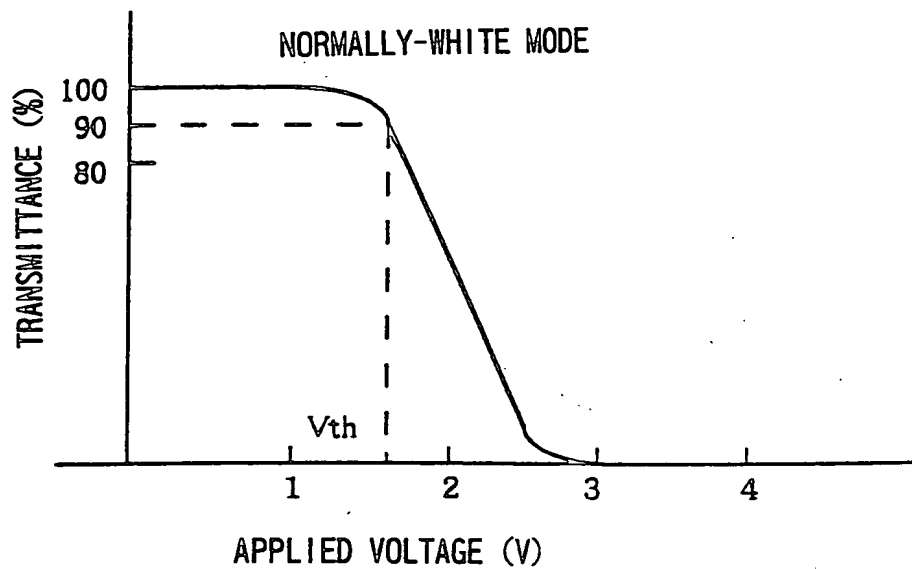


FIG. 10B

